What is claimed is:

1. In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card, a method for detecting the absence of a Phy Layer device on the back card and communicating said absence to the front card, said method comprising:

receiving, by the front card, a sensing signal from the back card;

if said sensing signal is a logical low, then coupling a IDSEL signal corresponding to a particular channel of said back card to said front card; and

if said sensing signal is not low, then decoupling said IDSEL signal from said front card and providing a logical low signal in the place of said IDSEL line.

2. The method of claim 1, wherein said sensing signal is received by the switching input of a tri-state buffer provided on said front card.

3. The method of claim 2, wherein said tri-state buffer further has an input and an output, said input and output being serially disposed on a IDSEL line corresponding to a particular channel.

4. The apparatus of claim 1, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy.

5. The apparatus of claim 4, wherein said front card and said back card are coupled via an MII bus.

6. The apparatus of claim 1, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

7. The apparatus of claim 6, wherein said front card and said back card are coupled via a TDM bus.

8. The apparatus of claim 1, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

9. The apparatus of claim 8, wherein said front card and said back card are coupled via a Utopia bus.

10. In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card, an apparatus for detecting the absence of a Phy Layer device on the back card and communicating said absence to the front card, said apparatus comprising:

means for switching disposed on the front card;

said means for switching being configured to receive a sensing signal from the back card, said sensing signal having a first and second state;

said means for switching being further configured to provide a predetermined signal to said front card responsive to said state of said sensing signal.

11. The apparatus of claim 10, wherein said means for switching comprises a tri-state buffer;

said tri-state buffer having an input, an output, and a switching input;

said input and said output of said tri-state buffer being serially disposed on said front card; and

said switching input of said tri-state buffer is configured to be coupled to said back card.

12. The apparatus of claim 10, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy.

13. The apparatus of claim 12, wherein said front card and said back card are coupled via an MII bus.

14. The apparatus of claim 10, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

15. The apparatus of claim 14, wherein said front card and said back card are coupled via a TDM bus.

16. The apparatus of claim 10, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

17. The apparatus of claim 16, wherein said front card and said back card are coupled via a Utopia bus.

18. An apparatus for detecting the absence of a LAN or WAN compliant device, said apparatus comprising:

a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card;

said front card further having a switch, said switch being serially disposed on a IDSEL connection corresponding to a particular channel on said front card, said switch being further configured to receive a sensing signal corresponding to said channel from said device; and

wherein said apparatus is configured to couple said IDSEL connection to said front card if said sensing signal is in a first state, and provide a low potential to said front card if said sensing signal is in a second state.

19. The apparatus of claim 5, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy.

20. The apparatus of claim 18, wherein said front card and said back card are coupled via an MII bus.

21. The apparatus of claim 20, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 framer/line interface.

22. The apparatus of claim 18, wherein said front card and said back card are coupled via a TDM bus.

23. The apparatus of claim 22, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

24. The apparatus of claim 18, wherein said front card and said back card are coupled via a Utopia bus.